Francisco Paulo de Aboim

Strategies of Assembly of Finite Element Sparse Matrices with GPUs and OpenCL

**Dissertação de Mestrado**

Dissertação apresentada ao Programa de Pós-graduação em Engeharia Civil da PUC-Rio como requisito parcial para obtenção do grau de Mestre em Engenharia Civil. Aprovada pela Comissão Examinadora abaixo assinada.

Orientadores:

Elisa Sotelino

Luiz Fernando Martha

Rio de Janeiro, Junho de 2012

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Francisco Paulo de Aboim

Graduou-se em Engenharia Civil na PUC-Rio em 2010...

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Abstract

Aboim, Francisco Paulo de; Martha, Luiz Fernando; Sotelino, Elisa. **A Finite Element Implementation with OpenCL**. Rio de Janeiro, 2012. Master's Dissertation - Department of Civil Engineering, Pontifícia Universidade Católica do Rio de Janeiro.

The paper investigates the implementation of the finite element method using the OpenCL (Open Computing Language). GPU computing is becoming increasingly popular because of its ability to efficiently perform highly parallel computations, such as vector and matrix operations. Current GPUs have approximately 100 times more computing power than a CPU because they work in lockstep using a pipeline model. However, GPUs are less flexible and require more care and patience in their programming. Furthermore, each graphics card manufacturer provides its own programming language. OpenCL is being viewed as the standard for heterogeneous platforms. Its development is supported by a consortium of major vendors such as Apple, Nvidia, AMD, Intel, Nokia, Motorola, and others. The finite element method is the most widely used method to solve complex computational mechanics and engineering problems. It involves matrix and vector operations in many of its phases and therefore is an excellent candidate for GPU computing. In this investigation, the use of OpenCL is explored to a maximum on the different phases of the method. Both code implementation and its optimization are discussed. Comparisons with an optimized implementation using a classical parallel processing implementation using OpenMP on a multiprocessor machine are provided.

**Keywords:** GPU computing, OpenCL, High Performance Computing, Parallel Finite Element Analysis

Sumário

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A Finite Element Implementation with OPENCL

Francisco Aboima, André Brabob, Elisa Sotelinoa, Luiz Fernando Marthaa

aDepartment of Civil Engineering, Pontifical Catholic University, Rua Marques de Sao Vicente 225, 22451-900 Rio de Janeiro, Brazil, fpaboim@tecgraf.puc-rio.br, lfm@tecgraf.puc-rio.br, sotelino@tecgraf.puc-rio.br, <http://www.tecgraf.puc-rio.br>

bDepartment of Civil Engineering, Fluminense Federal University, Rua Passo da Patria 156,  
24210-240 Niterói, Brazil, andrebrabo@vm.uff.br, <http://www.uff.br>

1. Background
   1. The CPU Architectures and the Road to Massively Multicore

The motivations of researching new programming models targeted at heterogeneous multicore systems are inherently tied to the motivations that led to the development of multicore systems. Moore's law is well known inside and outside the computing community for having been able to predict with remarkable accuracy back in 1965, in the celebrated and often cited article "Cramming more components onto integrated circuits" (G. Moore, 1965), that transistors on integrated circuits would double roughly every two years. This claim has gained such notoriety because, regardless of silicon price fluctuations, technological breakthroughs and investment in research and development it has held to this day. Not only did Moore predict this trend, but he also was able to envision what would be one of the greatest barriers processor manufacturers would face to keep up with the trend and postpone diminishing returns: heat generation. In the same article Moore poses: "Will it be possible to remove the heat generated by tens of thousands of components in a single silicon chip?” a question that lingered for decades while the growing problem was addressed by cooling solutions which got progressively more complex and expensive. In a few decades passive heat sinks evolved to active heat sinks (including fans to increase the heat exchange), copper heat tubes and a variety of fan designs to optimize air flow (fig).

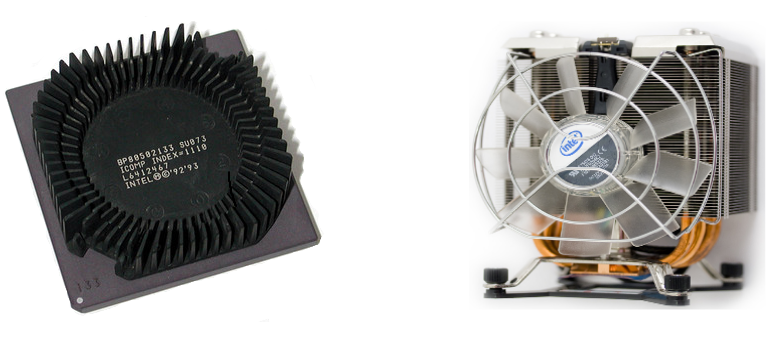


Fig x

We have now reached a point where current processor gates are around 20 nm wide (As in Intel's 22nm Ivy Bridge) or about 74 atoms of silicon wide (with prototypes being even smaller). When dealing with these dimensions, transistor gates have become increasingly susceptible to an effect defined in quantum physics as quantum tunneling. Quantum tunneling tells us that the smaller the barrier is, the greater the probability that an electron will be found on the other side of the barrier. Recently gates have gotten so small that this probability has risen dramatically and the loss of energy due to electrons tunneling through the insulator has become a barrier to further miniaturization, since energy loss translates into an even higher production of heat. The loss of energy due to these effects is commonly named *leakage*. During decades, the processor industry has been able to increase processing power by miniaturization and increasing clock frequency. During the last years, due to Leakage becoming an increasingly important factor, the industry has hit a frequency wall where further gains in processing power by increasing clock speeds are leading to a higher marginal cost, in terms of power consumption (fig). To deal with this, many techniques have been proposed, all of which lead to an increase in complexity, be it in the processor itself, compilers or shifted to the programmer himself (). As Microsoft researcher Herb Sutter put it: “The free lunch is over”. In the burgeoning mobile industry, where efficient use of processing power is paramount, industry players such as ARM which have for decades researched how to build efficient processors have gained a significant amount of market share due to the difficulty vendors are having in dealing with these setbacks.

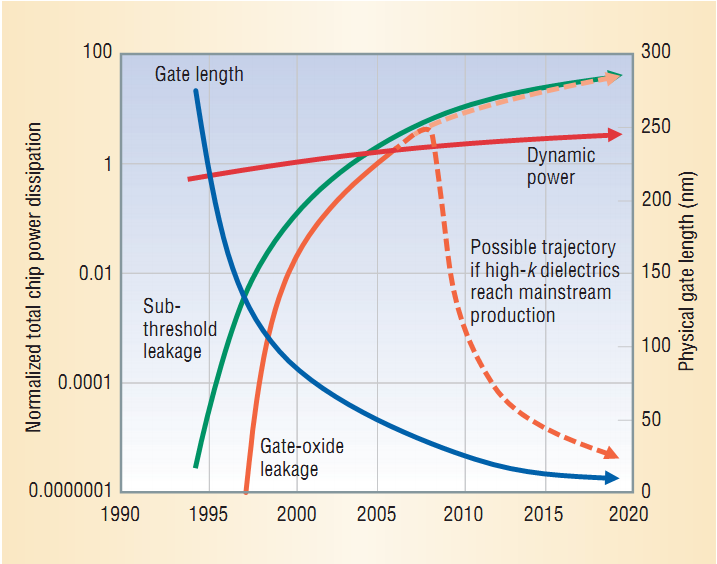


Fig x (Sung Kim, N. et Al.)

While the long awaited replacement for the common variants of the MOSFET (metal-oxide semiconductor field-effect transistor) technology do not arrive and contenders such as the graphene transistor, carbon nanotube transistor and other incipient exotic technologies are still being researched, albeit a long way from mass production. One of the solutions found to overcome these limitations was to simply pack more cores into a single processor which set the trend of the multicore era. This solution, although obvious, was not implemented at earlier stages because of one problem: almost all production code was designed with the serial programming model in mind.

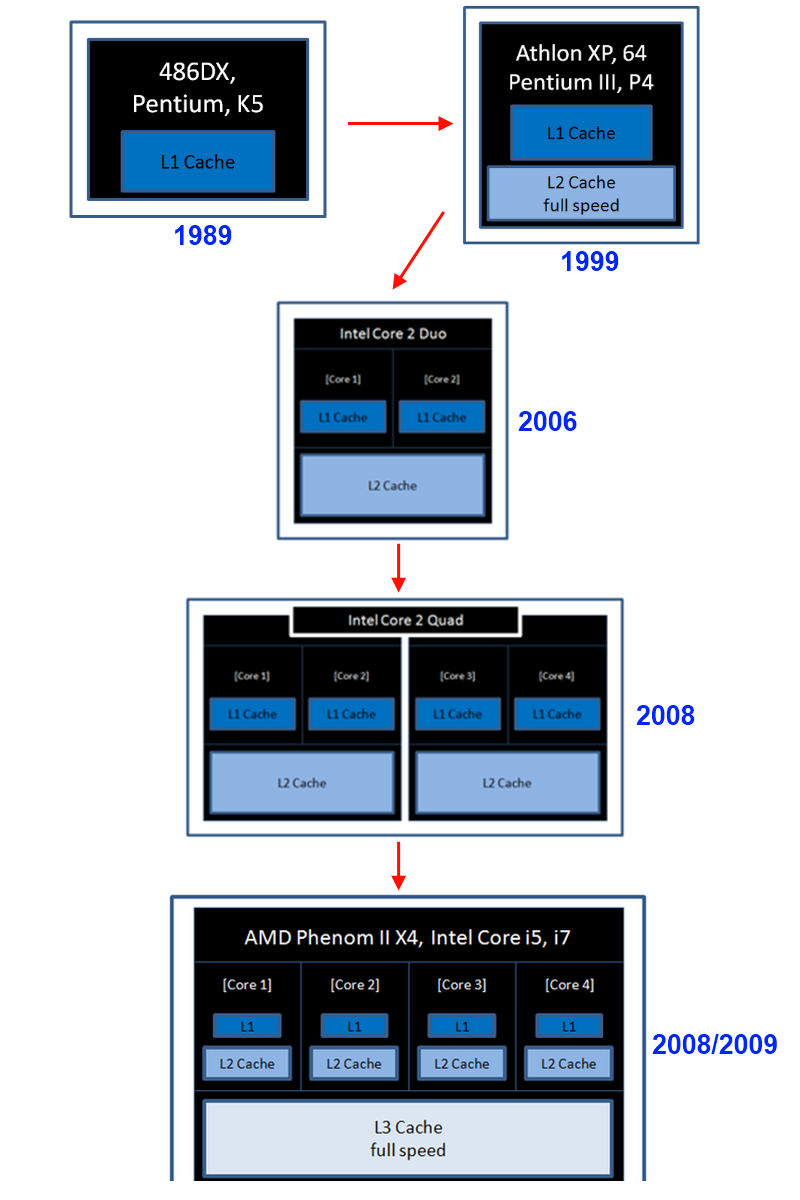
Such a fundamental hardware change meant that programmers now had to redesign their hardware and algorithms with a different mentality and the burden of having increasing computing performance from a piece of code was now partially passed on to the programmer, who could no longer depend on better compilers and faster processors to gain increased performance. Not only would serial code cease to run faster on newer generations of processors, but the code could actually see its performance degrade, since clock rates stagnated or even fell to be able to accommodate the extra heat produced by the addition of more cores. Still, clock speeds and transistor counts are not the only factors which affect processing power, and every possible avenue was explored.

One of the main factors is the number of instructions per cycle which translates roughly to the amount of work which is done per clock cycle. Unfortunately, the number of instructions per clock has hit its own wall [Stamatis Vassiliadis et al.] and has remained fairly constant in the past years. Not being able to achieve more performance out of instruction level parallelism (ILP), once an oasis for squeezing more performance out of processors, has led to focusing efforts at other programming models.

Another imperative factor for driving performance is memory speed. While processing power has kept up with Moore's law as described, memory speed has risen at a slower pace. This has made the spread between processing speed and memory access speed grow larger as the years went by and no new technology was developed that significantly increased memory access speed in a cost effective manner. Moreover, with the addition of more cores to processors, communication between cores has increased over previous models (Psota, J. et Al). Due to wire delay, this trend has obviated the necessity of exploring data locality, particularly in more recent years with the rapid increase in numbers of cores. Because of this, many of today's computational algorithms are not actually limited by processing capability but by memory bandwidth and speed.

Before processors started using cache as means to speedup processing, faster types of memory did exist and were available but at a much higher cost which made it impossible for them to hit mainstream production. The solution Intel first implemented on the i386 chip was to allow an extra space on the motherboard where a small amount of high speed memory could be connected to provide the processor with high speed memory access for whoever would be willing to pay for it. With compilers getting smarter and adapting to these changes, engineers saw that adding a small amount of cache to a processor could greatly increase the processing speed since all data was not used equally. As an example, while performing a task such as multiplying an n-sized vector by a scalar, the scalar is used n times while the vector is used only once. If the scalar were to be cached, the reading time would be an order of magnitude faster without the need to use high speed memory to store the whole problem's data. One would simply have to have space for a single float or double, normally a measly 4 or 8 bytes, a realization which prompted Intel to create the cache in the first place, given the high marginal gain of using a small portion of costly high speed memory. This architectural change was such a success that on the next family of processors, the i486 the cache started to be included on the same wafer as the processor. In modern processors the traditional architecture with one memory space was replaced by a hierarchy of different memory levels. AMD's Athlon XP and 64 and Intel's Pentium 3 and 4 added one more layer to the memory hierarchy with the addition of a larger but cheaper L2 cache. With the advent of the multicore architectures Intel's Core 2 Duo created an L2 cache which was common to both cores and therefore permitted sharing of cache memory between cores while the L1 cache was faster but core specific(for counters and such) which further impacted programmability. Current processors such as the Phenom X4 and the Intel core i7 have yet another added level of memory with cores having their own L1 and L2 caches, and sharing an L3 cache (fig).

One unintended effect was that the complexity of the compilers increased dramatically with this new type of memory. Compilers have to decide what to put in the cache, when to put it there - since even changing the order of execution of independent events can impact performance - and where (at what cache level) to write the information. The sharing of information on certain caches also created new possibilities for optimizing code by allowing parallel computing within the cache memory level. While compilers have evolved significantly over the last decades in terms of optimizing code, they are limited in what they know of the task at hand. If one were to have an algorithm with deterministic memory access it would be easy to outperform a compiler by planning ahead and manually decide which variables to store in the different levels of cache and by tweaking memory use to maximize bandwidth by sharing information at high speeds through the common memory cache. In this manner, many linear algebra libraries can achieve performance much higher than would be expected by running a naïve version of the routines in C or Fortran and letting the compiler do the work.



* 1. Vector Processors
     1. The Development of Vector Processors

The SIMD (Single Instruction Multiple Data) paradigm as described by Flynn’s taxonomy (Flynn, 1972) describes an execution model where the same instruction is executed on multiple units of data (words). A vector processor is an implementation of this model where, contrary to a scalar processor which operates on a single word, the same instruction is executed for N words, which can also be viewed as executing on a N-dimensional array of words. Immediately, we can identify that the instruction bandwidth will be much smaller since only one instruction read will be required for operating on N words and, therefore, the instruction read overhead will be 1/Nth of that of a scalar processor. Nevertheless, this will only happen if all N processors are actually processing useful information. Since vector processors execute in lock-step, i.e., all individual processors are required to concurrently perform the same operation, if the operation is not data-parallel or barely so, only one or a few of the processors will be used and unused processors simply operate on any data and have the result discarded, resulting in a less than optimal efficiency. Vector processors are, in essence, engineered to solve problems which are predominantly data parallel.

Given that vector architectures are only suited for a specific type of problem, widespread adoption only occurred in the 70’s with the infamous Cray-1 supercomputer. Besides being the first successful supercomputer to employ vector architecture, the Cray-1 was also ahead of time in that it employed individual registers for each vector processor and used a pipeline model, both of which are ubiquitous in today’s computers. One of the reasons for its success was that, like modern GPU’s, the Cray-1 could deliver a much greater performance compared to other supercomputers of similar price – for problems that were inherently data parallel.

While modern CPUs are not vector processors *per se*, vendors have added instruction sets over the years that make use of vectorization for added performance for specific operations with examples such as Intel's SSE/MMX and 3DNOW!.

* + 1. SSE and CPU Instruction Sets

A characteristic of the x86 architecture is that one of the ways vendors can deliver additional performance is by using wafer space for adding instruction sets. On the other hand, wafer space is limited and therefore there is a tradeoff between adding instructions or cache, for example. Adding instruction sets also increase chip complexity, but when they can be used, large gains in performance can be obtained. While the work can be done on the software side, instructions transfer the load to the hardware and usually accomplish the task in a fraction of the time required. Instruction sets exist for a diverse number of applications, from multimedia to 3D rendering (which recently has been dropped given that nowadays it is rare to utilize a CPU to process graphics). One of the most useful, particularly for scientific computing, is the Streaming SIMD Extensions (SSE) family of instructions which was born to address the shortcomings of the first SIMD instructions proposed by Intel, MMX. It has since then been expanded four times since the inception and is still in the process of being extended in new chips. The SSE family, as the name implies, is a SIMD extension which permits the processor to perform as if it were a vector processor, being able to achieve much better performance on parallel operations. This is accomplished by storing data in registers which possess faster memory access and by operating on these registers by using a set of instructions which can each operate on a whole vector of data in one clock cycle. Thus it is possible to compress into one cycle the computation that would take multiple cycles if done without vector extensions. It is also valid to point out that many times the way an algorithm is programmed makes is difficult to expose the vectorization potential to the compiler, which will result in suboptimal code. To trust the compiler for performance code is tricky and not straightforward, as sometimes even unrolling loops, aligning access and performing separate load/store operations as to expose vectorization will not be sufficient to guarantee the code will utilize the appropriate vectorization instructions.

Although considerable gains are possible using extended instruction sets, one other downfall which OpenCL addresses is that instruction utilization depends not only on the hardware where it is run but is also compiler specific. That means roughly doubling the lines of code if you want software that can be built on a windows compiler and GCC, for example. While using OpenCL makes the code capable of vectorization and compiler independent, for small functions which get called many times, such as in linear algebra libraries for CPUs, the overhead which OpenCL entails makes the code better suited for utilizing instructions directly. Although the resulting code may not be the most elegant, with conditional compilation to account for the platform and the necessity to port from one compiler to the other, for applications where performance is paramount, it is the best option.

* 1. GPU Architecture and the Development of General Purpose GPU Computing

With the advent of the programmable vertex and pixel shaders, developers were given the flexibility of creating their own code for customizing the rendering process to meet their needs. While most developers used this new technology for its original purpose, i.e. creating custom graphics effects or adding realism, it became clear that while the shader was made to operate on a vertex or pixel, any data could be treated as such and thus the GPU (Graphics Processing Unit) could be programmed to be used for any general purpose computation. With the rapid growth of the processing power of GPUs which quickly surpassed that of CPUs (central processing units) pushed by the highly competitive gaming industry, research began to appear that took advantage of the great and untapped pool of GPU resources. To process hundreds of linear transformations required by shader algorithms, state of the art GPUs possess hundreds of “small vector processors”, also called SIMD engines (fig) each of which contains a few ALUs. This means that even though GPUs in general operate with a smaller clock rate with regard to CPUs, current hardware is able to perform *thousands* of arithmetic operations per cycle, and frequently hundreds of special functions (sine, cosine, square root, etc.). It is valid to observe that comparisons regarding "processing power" are used rather loosely and can be taken to mean peak throughput (which is harder to achieve on a GPU), and this liberty was taken for the sake of comparison.

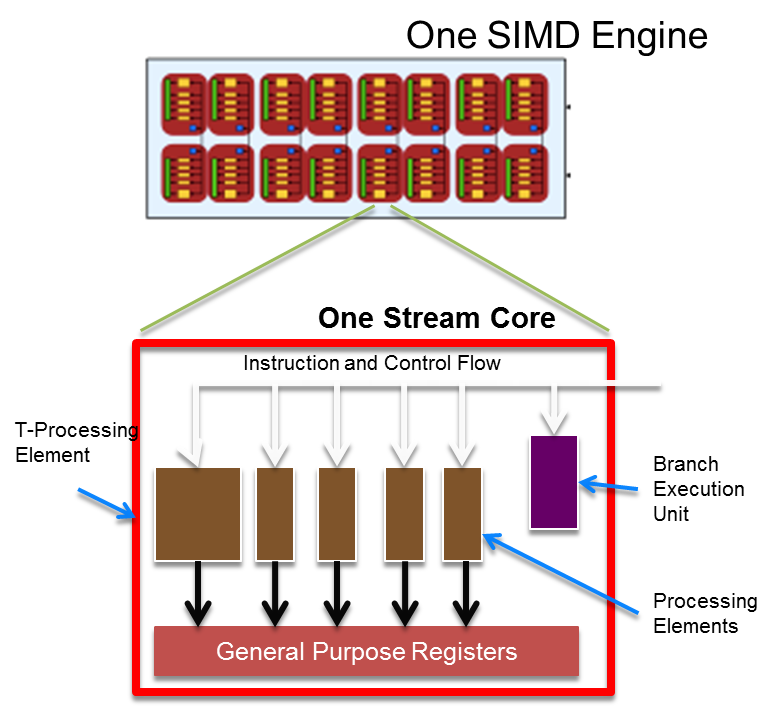


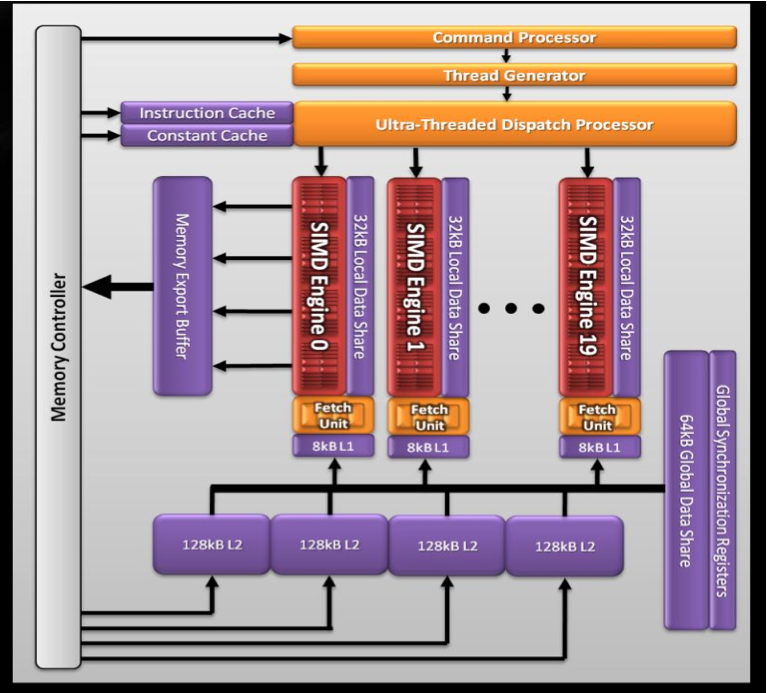
Fig.

Although the potential gains were high, so was the initial investment in learning to program for general purpose computation on a GPU. Initially only programmable in assembly, GLSL greatly increased the ease of programming shaders by raising the level of abstraction and offering the developer the ability to program his own kernels in C. While this was more practical than writing assembly code, GLSL was still a language written for shaders and not for performing general purpose computations on a GPU. This introduced some awkwardness in the process of programming because of the necessity of treating any piece of data which was operated upon as a pixel or vertex. Nevertheless, the ease of being able to program a shader in C, which along with Fortran is the most used language by the scientific community where performance is paramount, made this new technology gain much wider appeal. Furthermore, for many programmers familiar with the OpenGL API and the intricacies of managing buffers and the interface in general, the transition was facilitated, since the primary focus of the language was to extend OpenGL's capabilities and this was, after all, their targeted audience. A boom in research ensued which was primarily targeted at computer graphics but extended to other areas as well.

While the hardware continued to evolve, hardware vendors realized that vertex and pixel shaders had many overlapping functions. By joining the two shaders into a unified shader architecture, manufacturers were able to save wafer area and pack more transistors into the chip, while also being able to balance the computational load when one form or the other was being more heavily required - further increasing processing power. Also, this required that a new level of abstraction be introduced, since shader was to be used for vertices and pixels, further increasing the programmability of the GPU.

Nvidia and ATI, the only two large GPU manufacturers who managed to survive the intense competition, recognized the potential of this new niche and developed their own high level languages to facilitate the task of creating a program to run on a shader, commonly known as a kernel. Of the two languages created by Nvidia and ATI (AMD), respectively CUDA and Brook+, CUDA enjoyed the most hype and was embraced as the standard for GPU computing because of a gentler learning curve and higher level of abstraction which made the it more accessible, as well as Nvidia's capacity to quickly develop a functional and mature programming language for the GPU. The fallback was that CUDA and Brook+ were still vendor specific languages and therefore allowed no flexibility for porting code to other platforms. Also, while IBM entered the mainstream processor market by creating the acclaimed CELL BE processor for the Playstation 3, which was promptly recognized as a viable alternative to GPUs for massively parallel computationally intensive tasks and spawned the creation of a number of beowulf type clusters because of its low cost per FLOP (Floating Point Operation), IBM added yet another language to the growing list of languages tailored for the massively multicore era.

OpenCL was therefore created in an industry effort to standardize the programming for these different platforms. While each vendor would have his own implementation, since there was a standard they would have to adhere to, the portability to different platforms would be guaranteed. This was made possible because while the underlying hardware was completely different when dealing with a DSP (digital signal processor), CPU or GPU. In essence, what was needed was an abstraction to deal with programming for multiple cores, possibly hundreds, and to be able to manually manage the different memory hierarchies, mapping the hardware abstraction to a programming model (fig). OpenCL was conceived with this purpose, and has been constantly growing in adoption, posing itself as a potential new industry standard for heterogeneous programming.



The standard is supported by most of the large processor vendors, including the largest growing market segment of the industry, that of mobile processors for smartphones and tablets which can also greatly benefit from such a programming paradigm. It is also valid to note that by creating a high level language that gives the developer explicit management of the different levels of the memory hierarchy also greatly benefits the CPUs, which have taken a road similar to that of GPUs to be able to keep up with Moore's law: add cores and layers of memory (cache) to increase performance. The general trend towards multicore and hierarchical memory requires a different programming framework, one of which is OpenCL.

1. OpenCL
   1. Introduction

OpenCL is a standard defined by the Khronos Group, which is formed by a consortium of major players in the technological industry including hardware manufacturers, software developers and middleware vendors with the purpose of creating an open and portable API for accessing the capabilities of multicore systems. OpenCL provides a level of abstraction which enables the developer to write code for heterogeneous platforms consisting of CPUs, GPUs, APUs, DSPs and Accelerators (e.g. IBM Cell BE processor) within one unified programming model. Through the OpenCL programming language it is possible to write code based on the ISO C99 standard extended to write functions, called kernels, which execute on the device. Through the abstraction of the hierarchical memory present in modern GPUs and CPU with multiple levels of cache, OpenCL provides the capability of creating code which will take advantage of greater bandwidth some levels of memory provide to create optimized code without the need resort to vendor specific instruction language. Although programming in instruction language provides a greater level of control, using OpenCL in to program in C99 like language makes the code comparatively more readable and maintainable, besides being a cross-platform solution. A large number of resources on programming with OpenCL are available online and a few good books on the matter have been released [Benedict R. Gaster et Al., Heterogeneous Computing with OpenCL] [Aaftab Munshi et Al., OpenCL Programming Guide]. Only the minimum necessary for the comprehension of programming done in this work will be covered, for a more detailed description refer to the previous resources.

* 1. Execution Model

OpenCL works on the abstraction of a GPU composed of multiple compute units. The compute units are, in turn, composed of multiple stream cores which work as vector processors as shown in fig. The stream cores contain multiple ALUs and in some cases a SFU (special function unit) which can in turn also be considered “cores”. Since the underlying hardware is so different from that of a CPU, certain concepts such as that of a CPU “core” do not map directly between both architectures and the term “core” must be taken with a grain of salt. For that reason, the ALUs are called *processing elements* within the context of OpenCL (fig x).

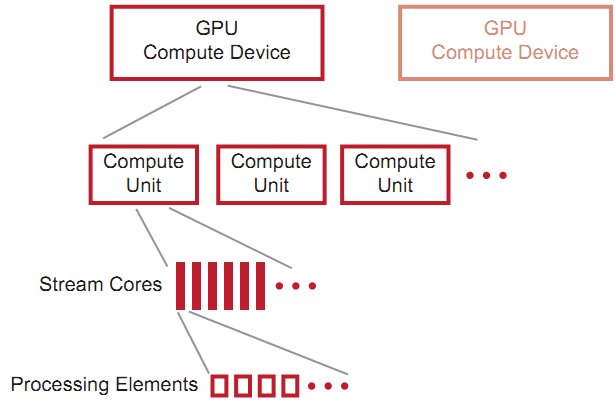
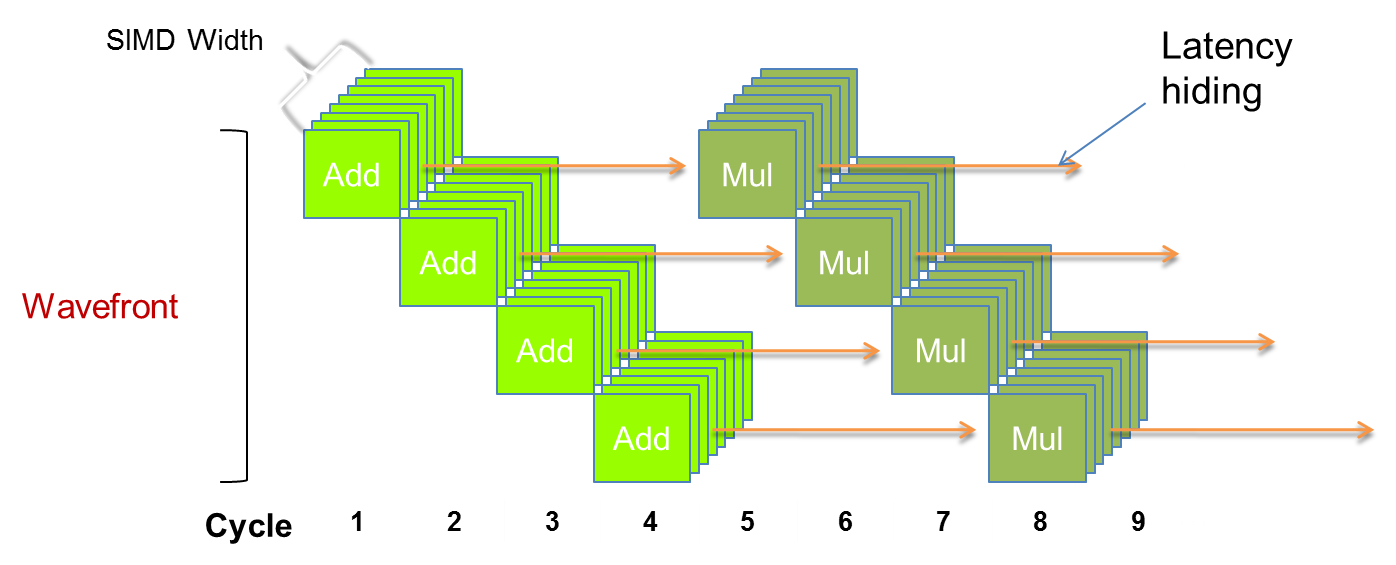


Fig x (AMD)

A kernel, as previously described, is basically and C function with some limitations, particularly with regard to memory management which is in large part deferred to the OpenCL library running on the host, and with access to special functions relative to the parallel computing model contained. Each compute unit runs an instance of this kernel, called a *work item* which is somewhat analogous to a CPU thread. Within a compute unit, all work items execute the same instruction. Since, ideally, hundreds of work items are generated and because of the common use with computer graphics and models, these work items are arranged in and N-dimensional grid, called *ND-Range.* Utilizing a 2D range for images, where each work item corresponds to a pixel, and 3D range for a 3D model, where each work item corresponds to a voxel, has its own benefits such as increasing cache hits by exploring data locality for certain algorithms, but in the context of finite elements utilizing a 1D range, i.e. a vector, suffices.

Work items are divided into groups called *workgroups.* A workgroup has access to common shared memory and synchronization directives which it can use to perform operations such as parallel reductions. The determination of the workgroup size also affects how private memory is distributed to each work item. The determination of work group size, therefore, has a large impact on the overall performance of the algorithm. Determining the best workgroup size is still something of an art and oftentimes counterintuitive, the best way being to simply test different variants. Work items are executed in fixed groups of work items, which depend on the hardware, called wavefronts. While wavefronts are determined by hardware, grouping is determined by software.

Due to characteristics of the GPU model, memory latency is preponderant factor in GPUs. To minimize the latency conundrum, GPUs pipeline work item execution so that while one work item fetches information from memory, other work items are executing. Up to four work items of the same wavefront can be pipelined on the same stream core. Performance is therefore dependent on keeping the pipeline full so that latency does not affect performance, a technique called latency hiding. An example of the pipelined execution can be seen in fig.



Fig

As a concrete example, one of the GPUs used for the test, the ATI Radeon™ HD 5870 HD has 20 compute units which each contain 16 stream cores. These cores each contain 5 processing elements adding up to a whopping 1600 processing elements. The wavefront size is 64 work items. While there is an immense added complexity, the theoretical peak throughput of this already outdated graphics card is 2.72 teraflops in single precision and 544 gigaflops in double precision (processing elements are linked together to perform double precision arithmetic leading to lower throughput). Nevertheless, as has been noted many times, achieving anything close to maximum throughput requires a special set of problems that can be parallelized into hundreds of different portions, preferably without the need of communication between these portions, and without branching. On most SIMD execution models, branching takes a heavy toll since lockstep execution does not allow diversion of execution paths and therefore should be avoided.

* 1. Memory Model

OpenCL contains four main memory domains: private, local, global and constant memory (fig.). Private memory pertains only to a work item and is not visible by other work items. Local memory can be shared between work items contained in a common work group and as previously mentioned provides synchronization directives. Global memory is visible by every work item. As in the different cache hierarchies in a CPU, there is progressively more memory on chip moving up towards global memory but memory access also increases by roughly an order of magnitude for each level.

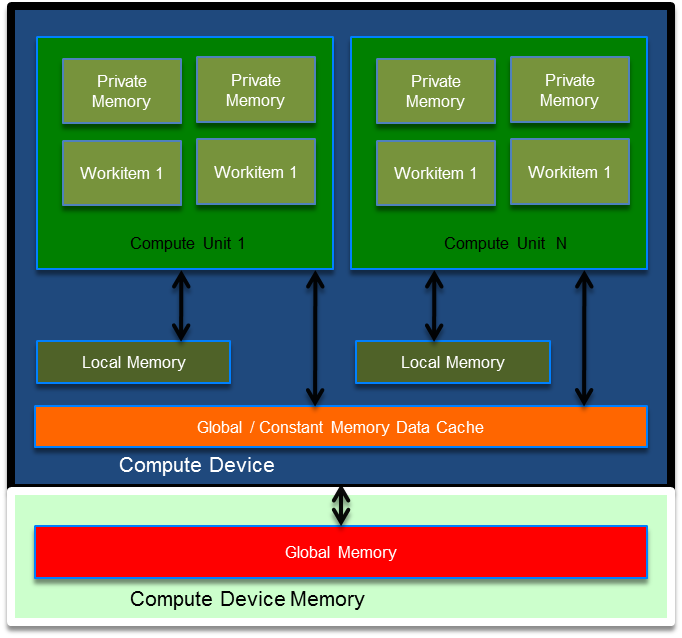


Fig.

The many layers the programming model contains, be it in execution or in memory management, are what make programming in OpenCL challenging. Wrapping one’s head around such concepts takes time to get used to, even for experienced programmers, particularly because the programming model is so alien to what programmers are generally used to.

1. Data Structures
   1. Sparse matrix storage Formats

Code for all sparse matrix data structures can be found on appendix X. Thorough discussions on the difference between data structures and which structures are more adequate for given problems and hardware architectures, particularly vector architectures, have been widely debated (P. T. Stathis, also Amer Wafai) and will not be restated here. Instead, only a succinct description of each format employed follows.

* + 1. Compressed Sparse Row

This particular implementation of the CSR format may have a few differing points from other implementation with regard to memory allocation, namely that each row has its own pointer which adds a memory allocation overhead but at the same time permits independent memory reallocations. In the context of finite elements this decision allows performance gains at the assembly stage when used in conjunction with mesh coloring, since independent memory management of rows to be resized in parallel, avoiding the issues of race conditions other formats have to consider. The strategy used was to create a C structure to hold each compressed row's data as follows:

typedef struct ROWdata {

fem\_float\* val;

int\* col;

int nNZ;

int maxSz;

} ROWdata;

The matrix is then represented by a vector of these structures which represent a compressed row. The advantage of utilizing this format for finite elements is that it allows rows to be reallocated in parallel, which faster if a matrix can be filled in parallel vis. other data structures which group all non-zeroes into one vector.

* + 1. Diagonal Format

The main advantage of the diagonal sparse matrix format is that given a regular band, this format can have a very small memory overhead, especially for stiffness matrices which have gone through a decent nodal reordering algorithm. Unfortunately the small gain in memory consumption is offset by poor performance and a much wider use of the CSR format.

* + 1. Ellpack Format

While the Ellpack format lost some ground with the demise of most of the vector supercomputers, with the return of the vector processing paradigm into scientific computing with GPU programming, other formats such as Ellpack-R (F. Vásquez et Al.) based on the Ellpack format have been devised to take advantage of vector processing and address prerequisites such as data alignment.

* + 1. Eigen Format

While not a separate format in itself, the Eigen sparse matrix library was added to the sparse matrix interface to have a library that performs well to compare to. While our formats were tailored for our problem and our needs, Eigen which is a general format performed well, particularly the dynamic format which has a memory overhead which is a bit larger than the regular format but has better performance regarding random insertion which is where most of the time is spent assembling a stiffness matrix. Another advantage of using the Eigen library is that since it is a header only library, it can be compiled with the code utilizing the same compilation optimization level as the other formats.

* 1. Search and Memory Access

Sorted arrays are commonly used to store indices and thus getting or setting information in the sparse matrix passes necessarily through these operations multiple times while assembling. Efficiently searching for the correct index is therefore a very important part in having a sparse structure that performs well. While understanding of Big O notation is necessary to understand the performance of an algorithm, relying solely on the limiting behavior of the algorithm as an optimization choice can yield counter-intuitive results if the nature of the problem is not taken into consideration. For problems with small N, for example, although in the long run a certain algorithm may yield better performance, setup costs may make the initial overhead trump the gains of a theoretically faster algorithm. As Donald Knuth points out “People often abuse O-notation by assuming that it gives as exact order of growth; they use it as if it specifies a lower bound as well as an upper bound” [Knuth, D; The Art Of Computer Programming vol1]. It is valid to point out that one could theoretically take Big Omega to be able to find a lower bound and from a theoretical perspective select the appropriate algorithm. Nevertheless, other factors such as caching, memory and bandwidth boundaries as well as the distinct performance of multiple memory hierarchies which are paramount for optimization are not captured by these models.

In the context of searching within a row of a matrix generated by the finite element method, row size is a function of mesh structure. The belief that selecting the “best” algorithm according to Big O notation in hopes of, at least, building a system that will scale well is in this case erroneous, since the algorithm will scale according to mesh structure and not problem size. Considering that elements connected to many other elements (e.g. “star” structure) are the exception rather than the rule, it would be wiser to program for the most common connectivity of each element. For each element type analysis was performed in order to find the impact of searching algorithms on sparse matrix performance. This analysis does not include OpenCL searching within the GPU, which has its own particularities and is discussed in the appropriate section. Differences between the different searching techniques have been discussed at length here: [<http://schani.wordpress.com/2010/04/30/linear-vs-binary-search/>].

* + 1. Linear Search

The traditional linear search algorithm was used as a basis to compare with other approaches used for searching an ordered array. The pseudocode for finding the correct place to insert a value in an array which returns and index is:

**FOR** position = 1 to length of vector

**IF** vector[position] >= value **THEN**

**RETURN** position

**END IF**

**END FOR**

We can then check if the value exists to discover if the value has to be inserted or modified or simply return that it does not exist in the case of a query. For small vectors, or in the case of sparse matrices for narrow bands, linearly searching across the vectors usually is faster than performing a binary search.

* + 1. Binary Search

The implementation for binary search was also used as a basis for posterior comparison with other versions. The pseudocode for the implementation is as follows:

**STORE** variable min set to zero, variable max set to length

**WHILE** (min < max)

**STORE** middle is average of min and max

**IF** (searched value > vector[middle]) **THEN**

**STORE** min is middle + 1

**ELSE**

**STORE** max is middle

**END IF**

**END WHILE**

**RETURN** min

* + 1. Linear Search with SSE

Using the SSE instruction set it is possible to speed up our linear search algorithm to search more positions per clock cycle. This can be done because utilizing special high speed CPU registers we are able to process multiple operations per clock cycle and, therefore, reduce the number of clock cycles necessary to perform the required operation. One of the downfalls is that aligned memory access is required to transfer the data efficiently to the registers, which impacts the requirements of the underlying data structure. Besides this, since up to 16 comparisons can be fitted into the registers, larger array sizes benefit the most from utilizing SSE linear searches. Second to all this, while the primary objective of writing optimal code is performance, utilizing SSE instructions makes the code harder to read, debug and maintain, especially considering that the code is compiler dependent and thus compiling for GCC would require extending the code with compiler directives. The SSE code utilized and compiled with MSVC was the following (description of the code was added as comments):

// Value to be compared is copied into 4 vector positions

\_\_declspec(**align**(16)) int v4[4] = {val, val, val, val};

const \_\_m128i\* v4ptr = (\_\_m128i\*)v4;

// Loads comparison values into registry

\_\_m128i key4 = \_mm\_load\_si128(v4ptr);

int i = 0;

\_\_declspec(**align**(16)) unsigned short res;

// Does search 16 elements at a time

for (i = 0; i <= len; i += 16) {

//

const \_\_m128i\* in0ptr = (\_\_m128i\*)&intvector[i ];

const \_\_m128i\* in1ptr = (\_\_m128i\*)&intvector[i + 4];

const \_\_m128i\* in2ptr = (\_\_m128i\*)&intvector[i + 8];

const \_\_m128i\* in3ptr = (\_\_m128i\*)&intvector[i + 12];

\_\_m128i in0 = \_mm\_load\_si128(in0ptr);

\_\_m128i in1 = \_mm\_load\_si128(in1ptr);

\_\_m128i in2 = \_mm\_load\_si128(in2ptr);

\_\_m128i in3 = \_mm\_load\_si128(in3ptr);

\_\_m128i cmp0 = \_mm\_cmpgt\_epi32(key4, in0);

\_\_m128i cmp1 = \_mm\_cmpgt\_epi32(key4, in1);

\_\_m128i cmp2 = \_mm\_cmpgt\_epi32(key4, in2);

\_\_m128i cmp3 = \_mm\_cmpgt\_epi32(key4, in3);

\_\_m128i pack01 = \_mm\_packs\_epi32(cmp0, cmp1);

\_\_m128i pack23 = \_mm\_packs\_epi32(cmp2, cmp3);

\_\_m128i pack0123 = \_mm\_packs\_epi16(pack01, pack23);

// Result is saved as a mask (fits more comparisons)

res = \_mm\_movemask\_epi8(pack0123);

if (res != 0xffff)

break;

}

int count = 0;

// To find position scans the bits of the resulting mask

if (res) {

unsigned long rb = 0;

\_BitScanForward(&rb, (unsigned long)~res);

count = rb;

}

return i + count;

1. Implementation of The Finite Element Method
   1. Determining the Global Stiffness Matrix

Determining the stiffness matrix is one of the main steps in performing analysis by the finite element method. Our version utilizes isoparametric finite elements, the most effective method for most practical analyses [bathe]. The global stiffness matrix is utilized to solve the matrix equation:

with which we can then insert boundary conditions to solve for the displacements. To first determine the global stiffness matrix, we first determine the local stiffness matrices of each element in the model and then assemble to a global stiffness matrix which represents all of the model's degrees of freedom. The element stiffness matrix can be evaluated as:

The work of calculating the integral is facilitated by using normalized coordinates, i.e. isoparametric elements, because when we perform a Gaussian numerical integration, we are always integrating in the same domain. To transform from natural coordinates to the general coordinate system, me must calculate:

Our corresponding pseudocode for the algorithm is, therefore:

**FOR** element = 1 to number of elements

**STORE** element Coordinates from node coordinates and element connectivity matrix

**FOR** gauss point = 1 to number of gauss points squared if in 2D, cubed if in 3D

**STORE** r,s,t natural coordinate values given the current gauss point

**COMPUTE** derivative of shape functions for current element type and r,s,t position

**COMPUTE** jacobian matrix given the element coordinates and derivative of shape functions

**COMPUTE** determinant of jacobian matrix

**COMPUTE** the inverse of the jacobian matrix given itself and its determinant

**COMPUTE** the derivative of shape function matrix in cartesian coordinates by multiplying the inverse of jacobian matrix by the derivative of shape functions in natural coordinates

**COMPUTE** B matrix by utilizing data in computed derived shape function matrix in natural coordinates

**COMPUTE** B transposed by transposing elements in B

**COMPUTE** CxB matrix by multiplying constitutive matrix C (given by constitutive model adopted) by strain-displacement transformation matrix B

**COMPUTE** temporary stiffness matrix by multiplying prior result, CxB, by B transposed

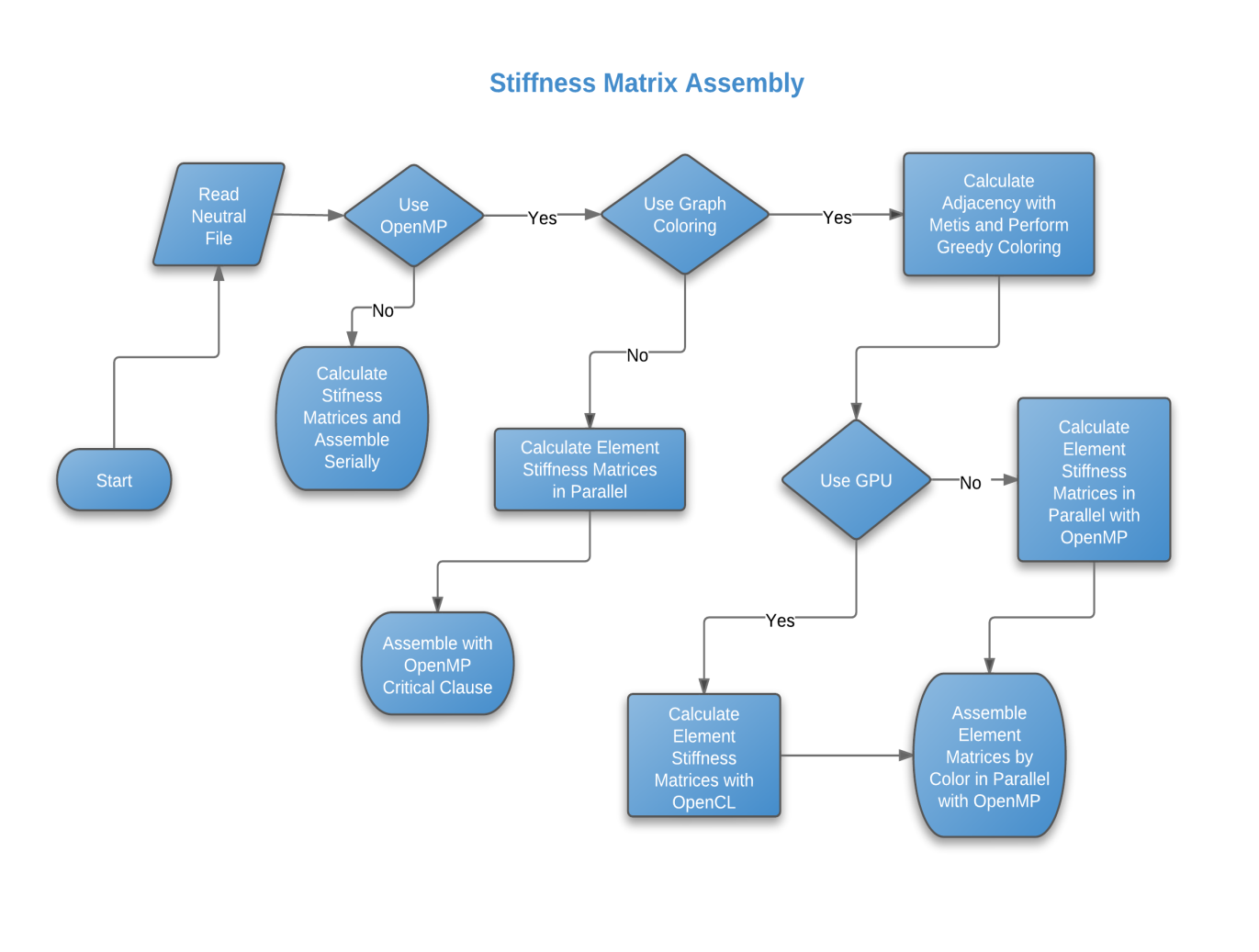
**STORE** in local stiffness matrix values calculating by adding the partical results of the numerical integration

**END FOR**

**STORE** in global stiffness matrix values of local stiffness matrix by assembling matrix into corresponding global degrees of freedom

**END FOR**

Since the in assembly process degrees the corresponding degrees of freedom are modified more than once, to parallelize this portion it is necessary to ascertain that concurrent threads are not simultaneously accessing the same element, which could lead to a race condition and yield erroneous results, e.g. two threads read the same value, increment the value by the amount that will be assembled, and then write to the same location irrespective of the work the other thread has done. To sidestep this problem it is possible to tell the compiler through OpenMP directives that a certain portion of the code should not be parallelized as covered in the OpenMP implementation section. Another possibility that maintains parallelism would be to calculate where these race conditions would arise, i.e. where elements have corresponding degrees of freedom, and “color” these elements with different colors. Therefore, while elements of different colors must be assembled serially, elements of matching color can be assembled without need for worrying about race conditions. Yet another option which is not covered in this text but which has been extensively discussed and which also yields good results would be to parallelize in the domain of the nonzeros(). The different paths possible which were implemented are all shown in the following workflow graph():



* 1. Parallel implementation using OpenMP

By utilizing OpenMP it is possible to have a considerable speedup in multicore systems without having to refactor a great quantity of code. With OpenMP it is possible to delegate and distribute work to different processors, while having control over locks, atomic decisions, load distributions and other features while maintaining a simple API.

One straightforward way to parallelize our code as referred to in () would be to compute the local stiffness matrices in parallel and then assemble to the global stiffness matrix. Care must be taken that race conditions do not affect the result, for while calculating the local stiffness matrices are independent calculations, when assembling the results race conditions may appear of two processors modify the same global degree of freedom at the same time. It is therefore necessary to utilize the CRITICAL construct from OpenMP to assert that only one thread performs this operation at a time. The resulting pseudocode would therefore be:

#pragma omp parallel for

**FOR** element = 1 to number of elements

**STORE** element Coordinates from node coordinates and element connectivity matrix

**FOR** gauss point = 1 to number of gauss points squared if in 2D, cubed if in 3D

Calculates local stiffness matrix

**END FOR**

#pragma omp critical

**STORE** in global stiffness matrix values of local stiffness matrix by assembling matrix into corresponding global degrees of freedom

**END FOR**

* 1. Parallel CPU implementation using graph coloring

By utilizing metis, a third party library to obtain a k = 1 graph coloring of the elements of the mesh by giving metis the elements connectivity. Metis then returns a colored graph which can be used to perform a quick greedy coloring and for a vector with all the elements for a given color. It is proven that there exists a coloring where the whole mesh can be colored in parallel in no more than n + 1 colors(), where n is the largest connectivity of all elements. This means that the mesh can be colored in no more than n + 1 steps, where each step may perform its calculations in parallel. Meshes with elements connected to many other elements are also a problem for other balancing methods and are usually discouraged during modeling. Nevertheless the presence of a few of these will not sufficiently impact the performance gain since for each of the added steps of an added connectivity there are usually hundreds of elements to be executed in each step which dilutes the added time of having to force a few sequential steps. All elements of a given color are executed in parallel for a given step, since elements that were given the same color have no degrees of freedom in common. This way it is possible to perform parallel loops over the elements without having to worry about race conditions in accessing the same element, as would happen with a dense matrix.

With sparse matrices certain particularities arise with regard to memory management since adding an entry sometimes requires reallocating an array which holds all nonzero values and therefore requires that the operation be performed by a single thread. This is a bottleneck of many sparse implementations. The compressed sparse row implementation, as described in the sparse matrix formats section, permits parallel access to rows and with graph coloring we are guaranteed that no two shared degrees of freedom are accessed concurrently. This way we can modify values and reallocate sparse compressed row matrices without having to worry about race conditions. The pseudocode for the parallelized version using graph coloring is as follows:

**FOR** color = 1 to number of colors

**#pragma omp parallel for**

**FOR** auxelem = 1 to number of elements with this color

**STORE** find current element based on elements for current color and auxelem index

**STORE** element Coordinates from node coordinates and element connectivity matrix

**FOR** gauss point = 1 to number of gauss points squared if in 2D, cubed if in 3D

Calculates local stiffness matrix

**END FOR**

**STORE** in global stiffness matrix values of local stiffness matrix by assembling matrix into corresponding global degrees of freedom

**END FOR**

**END FOR**

* 1. Parallel implementation in OpenCL

The parallelization in OpenCL was made calculating each element’s local stiffness matrix in parallel and assembling on the host device with the CPU utilizing OpenMP and graph coloring. The only difference between the assembly of the local matrices calculated by the GPU and the that of section 3.3 relative to the CPU is that while in section 3.3 the assembly was performed after each local matrix calculation the GPU code passed back a vector with all of the sparse matrices calculated and subsequently performed the assembly in the same manner. This implementation can be scaled to larger problem sizes/distributed systems easily by assigning the calculation of local stiffness matrices to different GPUs and performing the assembly of sub-blocks of local matrices by the host. Furthermore, for a given color multiple hosts can perform assembly in parallel and while GPUs are busy, given that proper care is taken to avoid race conditions regarding memory allocation (providing critical sections or preallocating matrices by counting nonzeros which can be done by third party libraries such as METIS). Different implementations exist such as utilizing a degree of freedom, i.e. a row/column of the sparse matrix as the domain of parallelization, or by nonzero which were very well documented and discussed (Cecka, C. et Al.).

* 1. Setting Boundary Conditions

Given the focus on performance and optimization, boundary conditions were enforced using the penalty method and heuristics such as the “Square Root Rule” [Felippa, Carlos; Introduction to The Finite Element Method]. While it is clearly not the best option in terms of numerical accuracy, this step does significantly affect the overall running time, and thus is not a primary concern regarding performance.

1. Results